

**Amendments to the Abstract:**

Please replace the Abstract with the following rewritten Abstract:

--~~The present invention provides for a~~ A register controlled delay locked loop having an acceleration mode ~~for improving accuracy to be correspondent~~ corresponding to an increase of the operation speed of a memory device~~[[.]]~~ is used to improve accuracy. ~~For this object, in the present intention, the~~ The register controlled delay locked loop includes a delay line, a delay model, a delay ~~means,~~ block, a first phase comparator, and a second phase ~~comparators,~~ comparator, a mode decision ~~means,~~ block, a shift register control ~~means,~~ block, and a shift register.--